Notice of Allowability	Application No.	Applicant(s)	
	10/655,580	HAKUSHI ET AL.	
	Examiner	Art Unit	
	D. I. Lee	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/12/05*.

2. ☒ The allowed claim(s) is/are *2-5 and 8-11*.

3. ☒ The drawings filed on *05 September 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Receipt is acknowledged of the Amendment filed 12 August 2005. Claims 1 and 6-7 have been canceled; claims 2-5 and 8 have been amended; and no claims have been newly added. Currently, claims 2-5 and 8-11 are pending in the application.

Allowable Subject Matter

2. Claims 2-5 and 8-11 are allowed.

3. The following is an examiner's statement of reasons for allowance:

Shinohara [US 6,523,755 B2] discloses a semiconductor memory device having a flash memory as a first memory, which is non-volatile, and RAM as a second memory having random access function. The first and second memories contained in one package (i.e., multi chip package), and semiconductor memory capable performing internal data transfer between the first and second memories, wherein the second memory has an internal data transfer control signal that controls the internal data transfer and an external transfer control signal that controls data transfer between an external CPU and the second memory (i.e., the operation of RAM controls the destination of the data transfer by determining whether data sent from CPU to be access to the flash memory or directed to the pseudo-SRAM of RAM), the second memory incorporates a controller (a flash I/F circuit and a bus controller circuit combine) that controls data access to the first and second memories, and when an access to the second memory requested from the external CPU during the internal data transfer (i.e., when the status is set to busy state), the controller controls the internal transfer control signal so that the internal data transfer is suspend (i.e., the controller controls the data transfer between the RAM and the flash memory by selecting one of the memory to read or write, thus, the internal data transfer is clearly interrupted or suspend when the controller selects the pseudo-RAM for data transfer is

suspend). Wherein the memory region of the second memory having a dual port function (i.e., connecting CPU and a storage flash memory) and is divided into plurality banks (plurality of registers and buffer).

One of ordinary skill in the art would not have been motivated to modify the teachings of Shinohara, alone or in combination with other references, in order to provide the semiconductor memory device with the specific function of the controller, such as outputting a wait signal to request the external CPU to wait for access when the internal data transfer is suspended, resuming the internal data transfer when CPU doe not access the second memory for a predetermined period during suspension, storing a bit that indicates a command for the suspension of the internal data transfer from the external CPU, and automatically transferring predetermined data stored in the first memory to a predetermined region in the second memory when the power of the semiconductor memory device is turned on, as set forth in the claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to D. I. Lee whose telephone number is (571) 272-2399. The examiner can normally be reached on Monday through Thursday from 5:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. I. Lee
Primary Examiner
Art Unit 2876